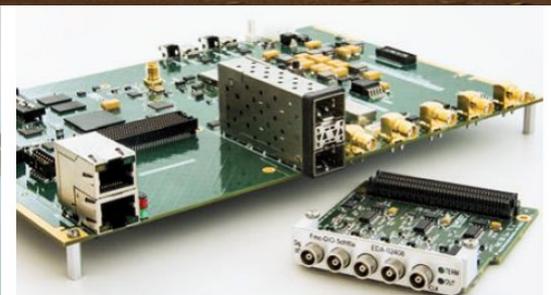
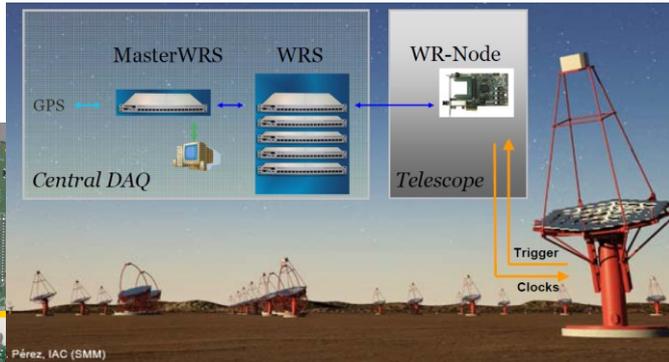
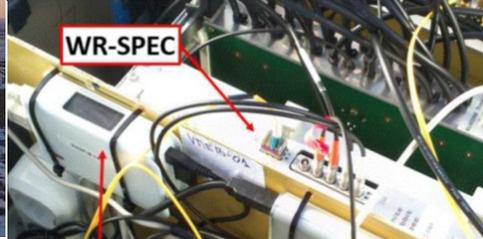


# Modern Timing Concepts for Astroparticle Physics

Ralf Wischnewski (DESY)



*Workshop on a Wide-FOV Southern hemisphere  
TeV gamma ray observatory, Puebla, 12.11.2016*



## Disclaimer:

- This talk is not a general review on Timing  
Focus is on the “new fashionable system”:

WHITE RABBIT (WR)



## Will answer this question:

- *“I bought a WR-Kit.  
Nice - it works for synchronization !  
Am I done ? ”*

## Executive summary:

- *There is One and Only One Timing System for APP*
- **But:** You bought a ‘Mercedes’ . It can play music, but it can also drive !



- **Precision timing in Astroparticle and Particle Physics Experiments**
  - Requirements, design principles
  - Avoid custom systems by using a “standard technique”
- **White Rabbit : an new technology for time-transfer**
  - Basics
  - Pro's and Pro's ( no Con's )
- **White Rabbit in operation: experience with Tunka-HiSCORE**
  - Experience over 2012—2015
- **Conclusion: make more of WR than only distributing PPS**

For more details see:

WR-HiSCORE: ICRC2013 (RW #1146, #1158, #1164)

ICRC2015 (RW PoS (1041) )

9<sup>th</sup> WR Workshop, Amsterdam, March 2016,

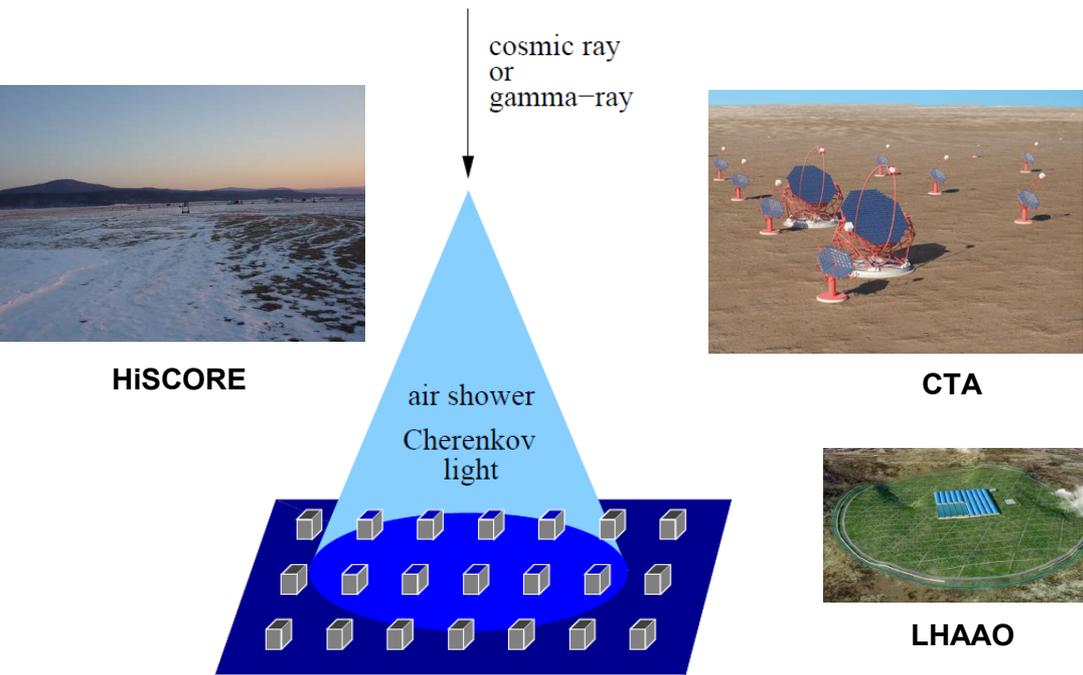
CERN-WR: <http://www.ohwr.org/projects/white-rabbit>

Thanks to my collaborators

M. Brueckner (PSI), A.Porelli (DESY)

# Large-scale Astroparticle Experiments ...

- > Detectors are distributed over large areas  
e.g. Sensor stations, Cerenkov Telescopes, Water-Tanks, Ice Tanks, DOMSs/PMTs
- > Measure: temporal arrival pattern of light-/radio-flashes/particles...
  - Examples: IceCube, Km3Net, CTA, HAWC, HiSCORE, LHAASO
- > Area:  $\text{km}^2 \dots 100\text{km}^2 \dots$
- > Timing precision: governs physics performance  
(sub-) nanosecond precision (sensor, media)



# ... and Timing (Trigger) concepts

## Centralized Arrays

Some large-scale AP experiments still do (like in compact accelerator experiments) :

- (1) measure times against a central reference signal ('*common stop*')
- (2) trigger at a central place (confirming the detector trigger-request signals).

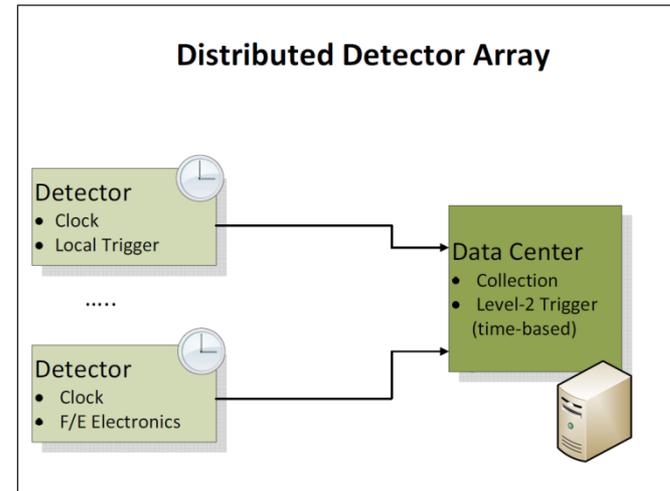
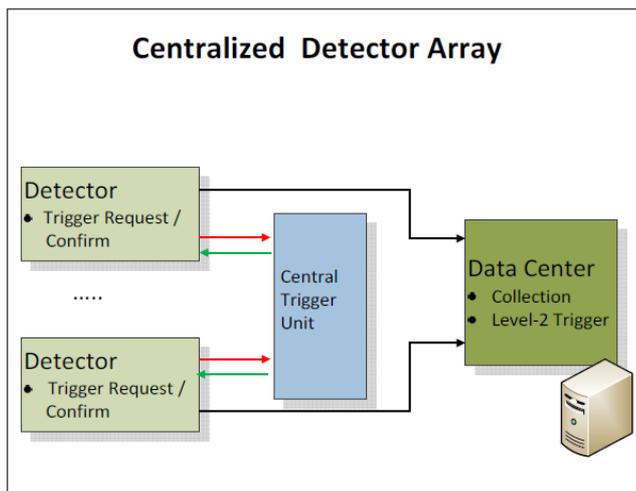
This "central triggering" can contribute to large dead-times, and analog-buffer depths.

## Distributed Arrays

Instead - with a **precision clock** in each detector, locally triggered sub-events can be send to a digital central processing unit (bandwidth and trigger-selectivity permitting).

This allows for complex array-triggering procedures, and low dead-times.

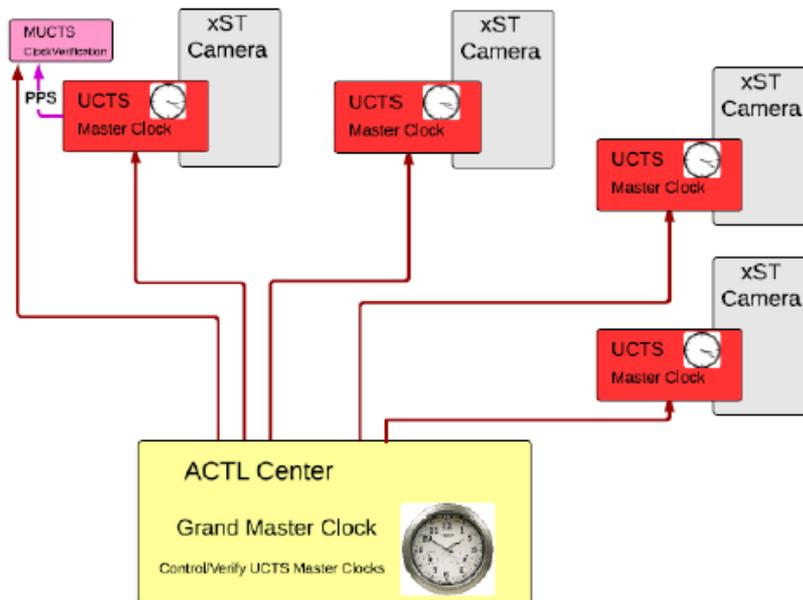
→ Clock reliability and precision is a system-critical parameter.



Each detector has a precision clock.

# Timing : Distributed Clocks

- Generic example: the array of CTA-cameras (or any other detectors)
- Each Camera has a precision clock, located on a Timing Card (UCTS).
- All clocks are autonomously synchronizing with the GrandMasterClock.
- Inter-Clock deviations are of  $o(200\text{ps})$  rms



- ➔ The array acts like a time machine, ie. must be able at each camera to either
- (A) measure (timestamp) an “event occurring”, or to
  - (B) generate an “calibration event”, ie. issue a clock-driven timesignal to camera.

# Technical Realization: White Rabbit



WR is a fully deterministic Ethernet based network for data transfer and synchronization.

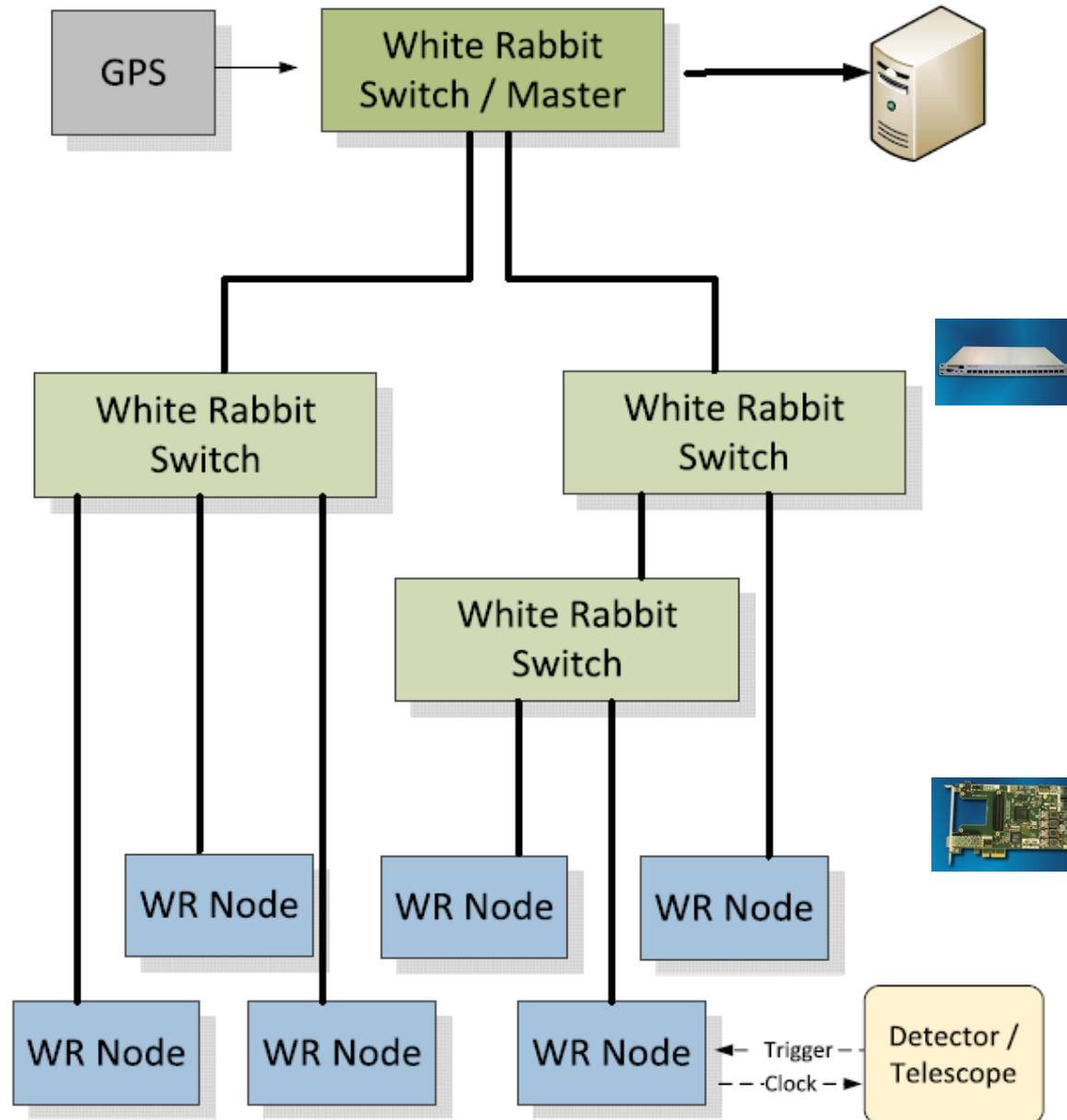
Extension of PTP. Uses proven 1GbE fiber technology.

A WR network is made of

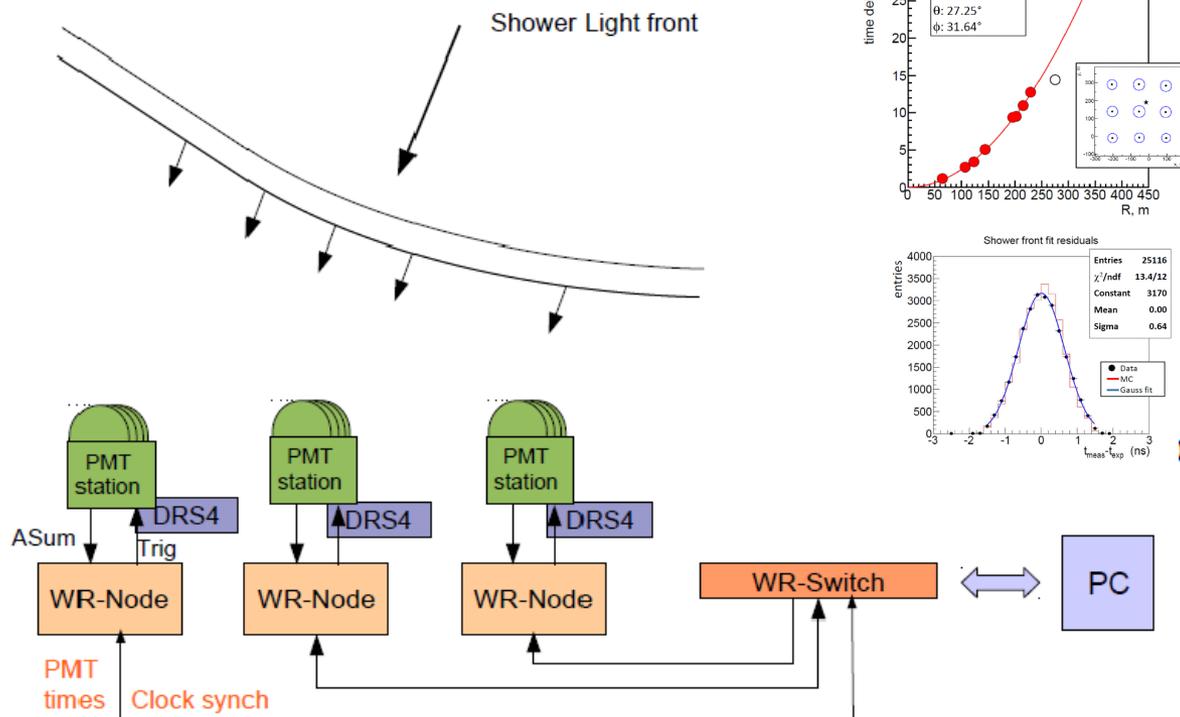
- ClockMaster (MasterSwitch+GPS)
- WR-Switch network
- WR-nodes with synchronized clock
- Standard GbE fiber connections.

Parameter:

- Accuracy <math>< 1\text{ns}</math>, Precision  $\sim 20\text{ps}$
- Fiber links of 10km ..... 60-80km.
- >1000 nodes.



# BonusSlide. Build your own nsec-DAQ



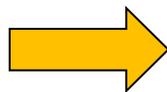
## Note:

This is an array-trigger free setup ! All detectors run standalone.  
Out-of-the-box !

Allows for true-online data treatment at array-level (Trig/Filter/...)

## Ingredients:

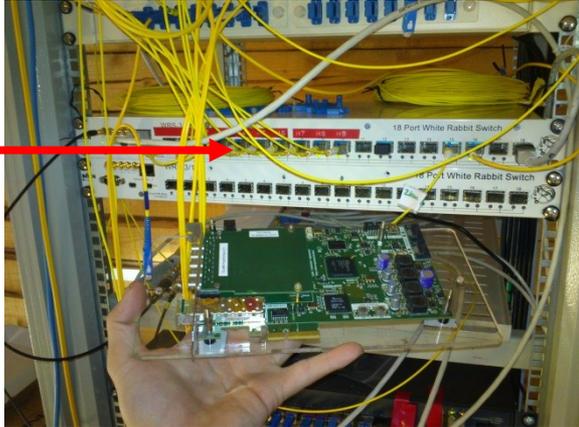
- Detector stations (PMTs...)
- 1x WR-SPEC per station (& your firmware)
- Fiber cable to WRSwitch



- Collect nsec-timestamps on your Laptop/PC
  - Reconstruct EAS wavefront ...
- (Optional: use DRS4/EB boards for pulse-sampling)

# White Rabbit: The Hardware Components

## WR Master: WR Switch



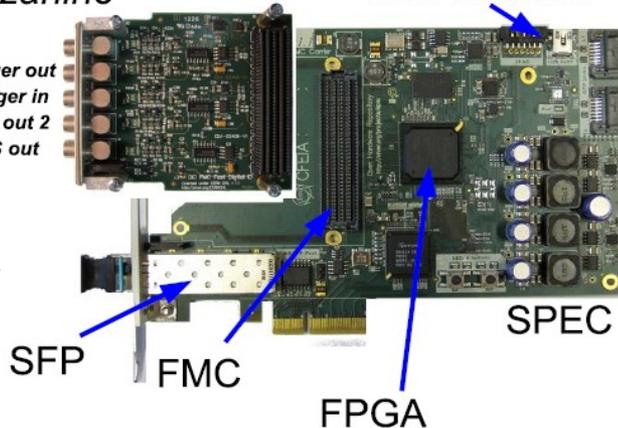
1Gbit fiber

## WR-Node: SPEC card

FMC DIO  
mezzanine

Trigger out  
Trigger in  
PPS out 2  
PPS out

USB terminal



SFP

FMC

FPGA

SPEC

## The WR Switch:

The synchronization master, connects to up to 17 WR-Nodes.

## A WR-Node: SPEC

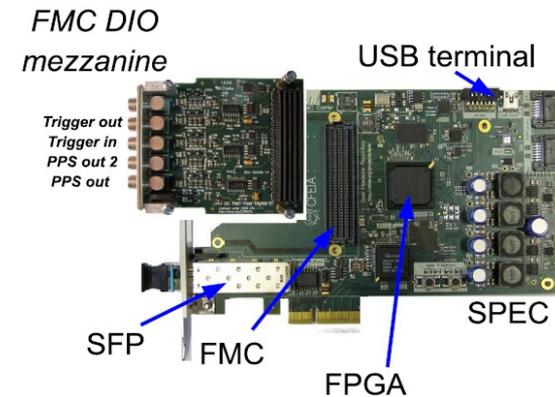
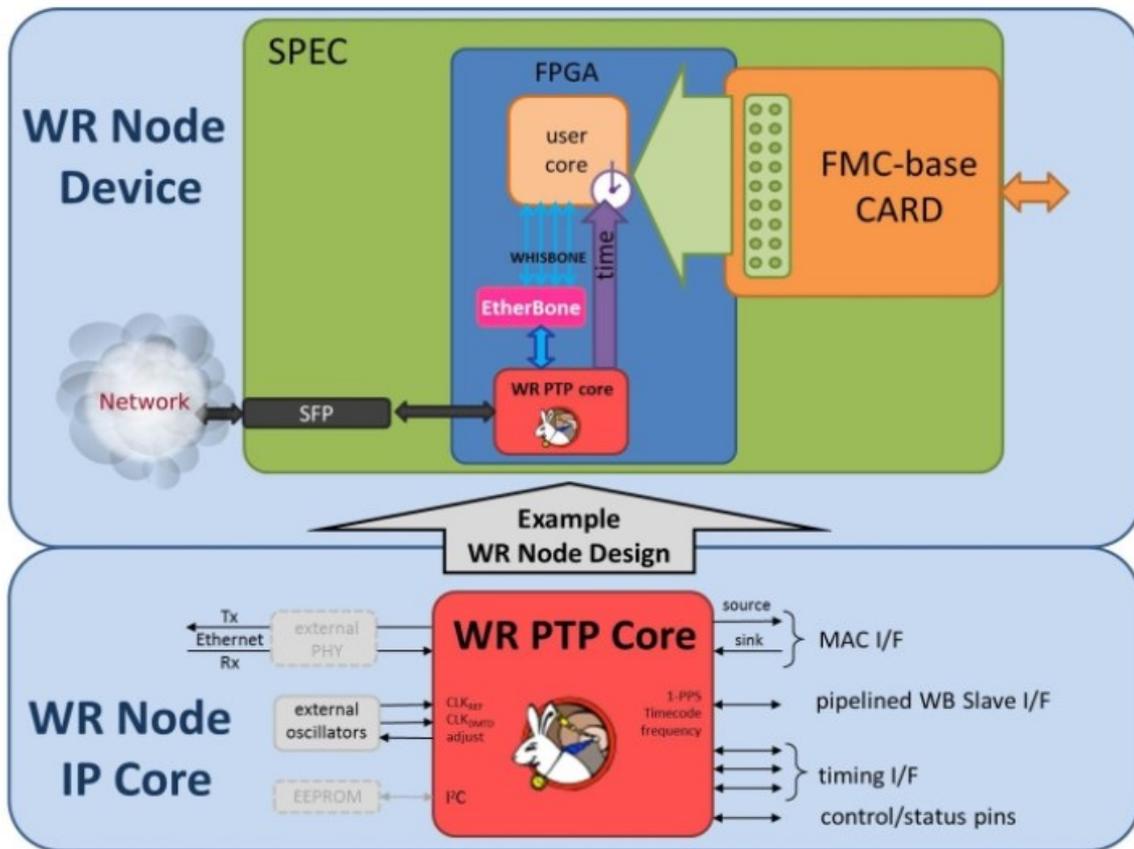
(“Simple PCI FMC Carrier”)

Spartan-6 based PCI-size card  
1x FMC (Mezzanine)  
1x SFP (WR fiber)

(the WR-Node workhorse since 2011)

(It's the WR-Node that needs experiment specific implementation)

# An example WR-Node



( example: WR SPEC )

# White Rabbit - Why is it attractive ?



WR is

- Supported by an active core-team @CERN,
- Planned for the LHC accelerator upgrade
- Growing participation from industry.

First astroparticle applications (“reference”) are underway now (e.g. LHAASO, HiSCORE). Results are very encouraging.

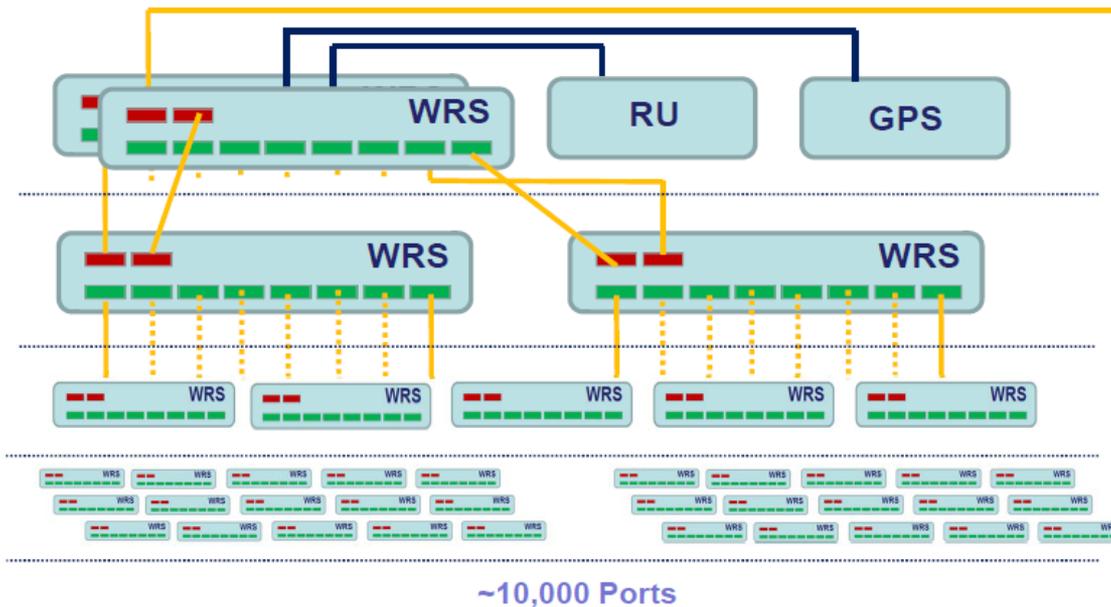
## Advantages :

- > Development for CERN & GSI accelerator complex; much external interest
- > Open Hardware & SW Project; peer reviewed; fully transparent to the user. Adapting to a use-case is easy and supported.
- > Hardware is commercially available (growing #companies),
- > WR Standardization is planned for Eth-PTP (IEEE1588...) in 2018
- > A guaranteed large user community: it will be a well debugged system ... !

# WR - Applications : LHAASO

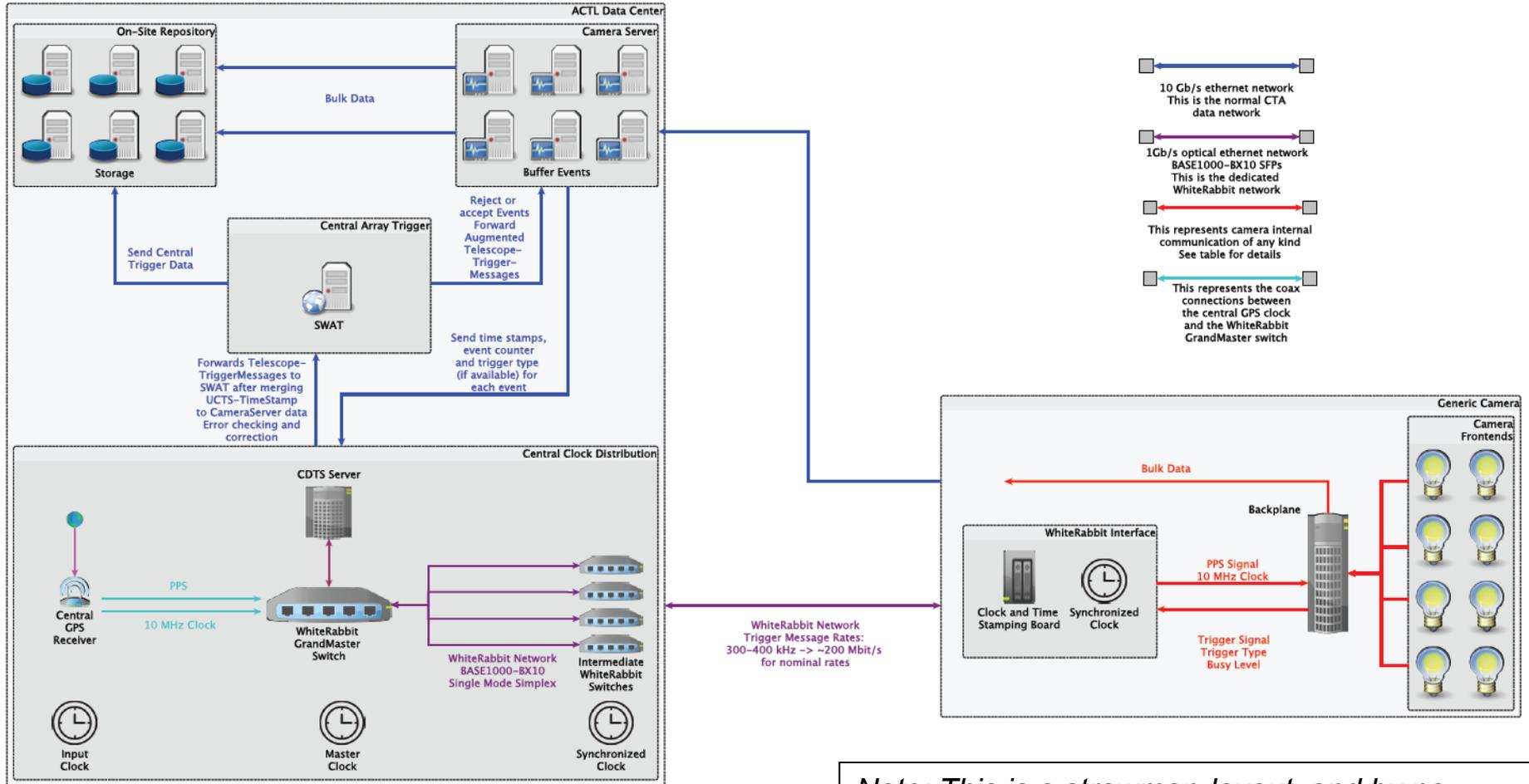
LHAASO : ~10000 nodes to be synchronized.

Test setups running.



G.Gong, ICALEPCS, 2011,  
ICRC2015, ....

# WR – Applications: CTA Telescope Timing & ArrayTrigger



*Note: This is a strawman-layout, and by no means final.*

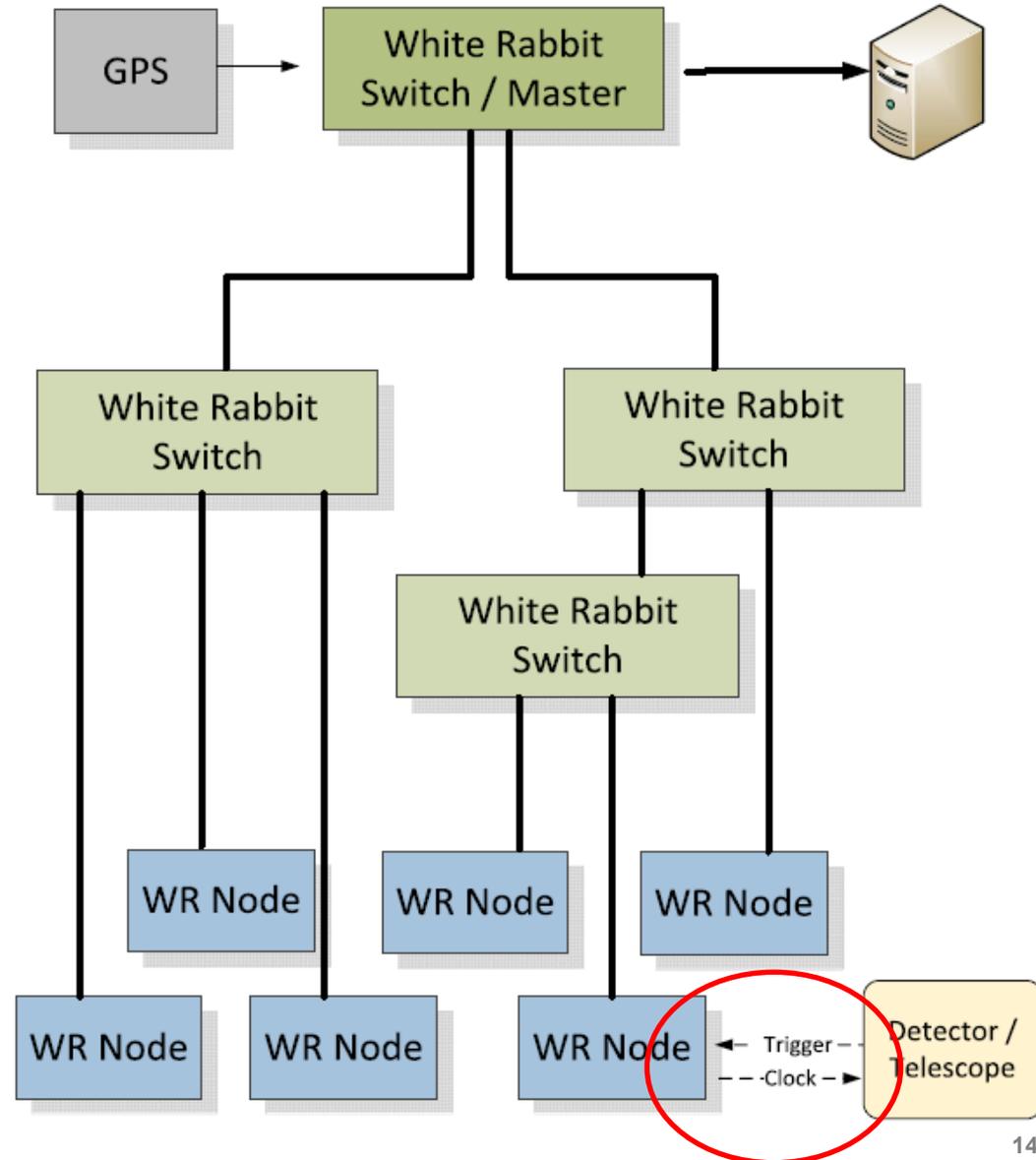
*CTA is discussing the data-flow concept and network architectures; since 2013.*

# ... and Timing : Using Distributed Clocks

AP experiments must act like a time machine, ie. at each detector being able

- (A) to measure (ie. timestamp) a “local event occurring”, or
- (B) to generate an event, by issuing a synchronous (to all detectors) signal.

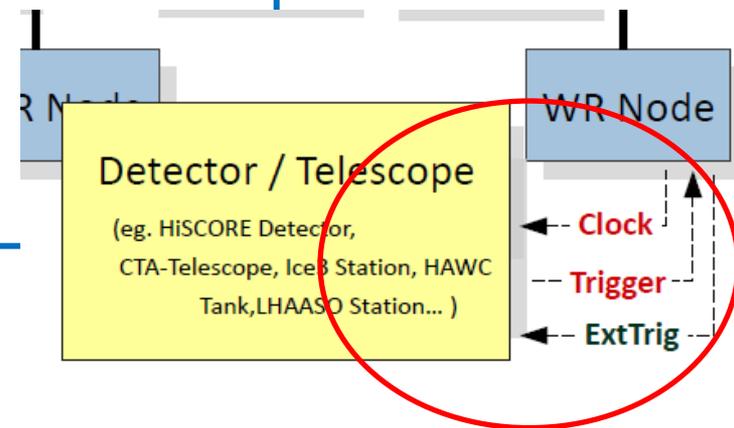
→ WR is a natural technique to be used for this.



# Detector and WR-Node : Baseline Interface

Functionality:

- WR-Node → Detector : Clocks ( PPS / 10MHz )
- Detector → WR-Node : Trigger ( edge )
- WR-Node → Detector : External Trig Pulses
- ...



Comments.

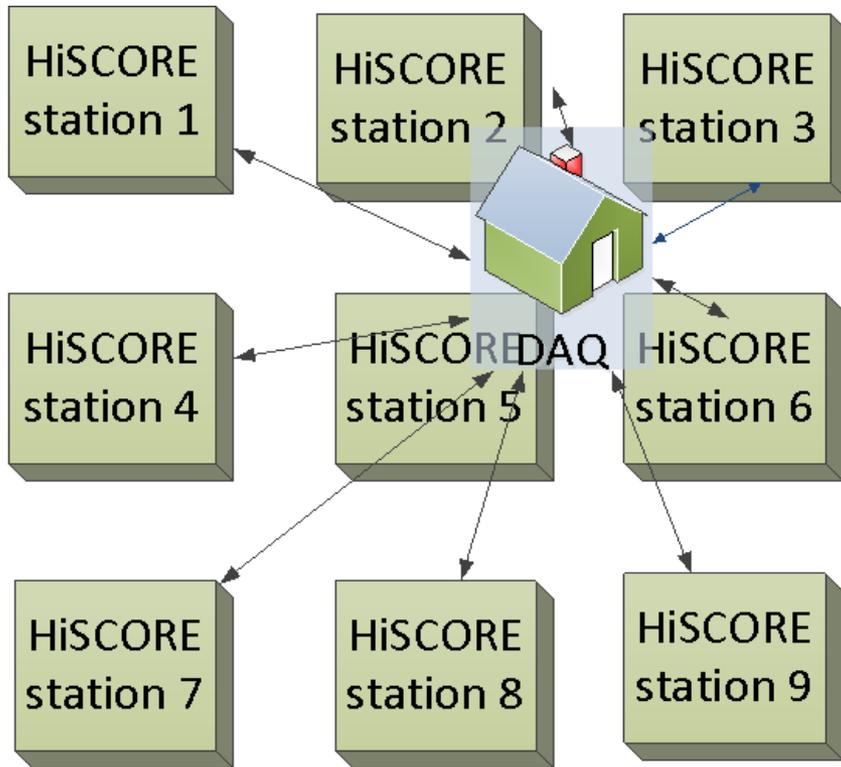
(1) TriggerTimes are generated both on detector and WR-Node for each event.

This (time/counter) redundancy can be used to verify clock stabilities and data integrity: **“DoubleClock/DoubleTimeStamping architecture”**

(2) Another request : Is in-situ verification of clock-performance possible ?

Allow for operation of a **Monitoring-WR-Node** at each detector, that cross-stamps the PPS. Cheap&sufficient; can be limited to verification and debugging phases.

# HiSCORE - Experience with White Rabbit



First prototype array: in 10/2013

$$A = 0.3 \times 0.3 \text{ km}^2$$

Each station detects Cherenkov light with 4 PMTs.



For precise shower direction reconstruction sub-nsec precision for arrival-timestamps at each station.

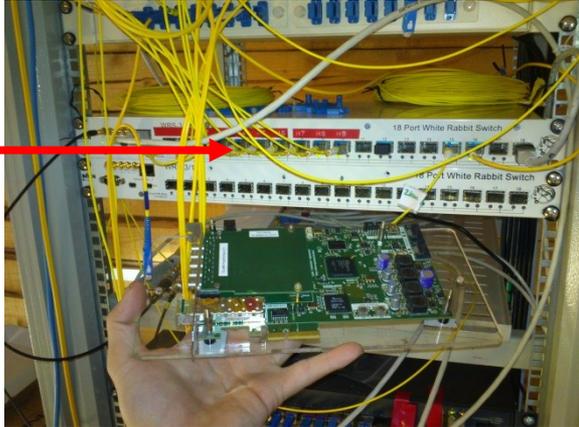
Prototyping with HiSCORE-9: Optical Stations / DAQ / Timing / ...

Main Results:

- Air-Shower reconstruction
- Timing calibration by external LED

# HiS-9 Station: The SPEC as the WR-Node

## WR Master: WR Switch



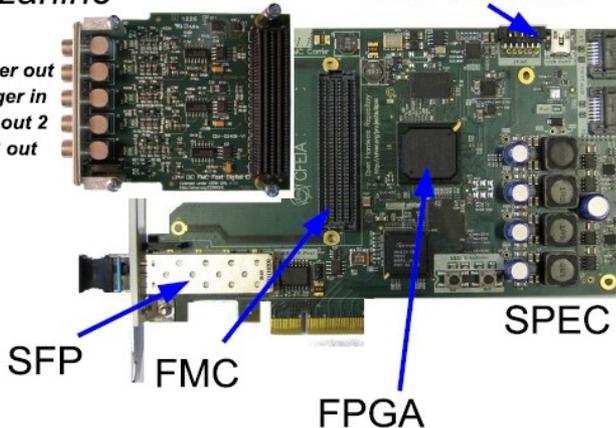
## 1Gbit fiber

## WR-Node: SPEC card

FMC DIO  
mezzanine

Trigger out  
Trigger in  
PPS out 2  
PPS out

USB terminal



SPEC = "Simple PCI FMC carrier"

Spartan-6 based PCI-size card  
1x FMC (Mezzanine)  
1x SFP (WR fiber)

The workhorse for WR (2011-...)

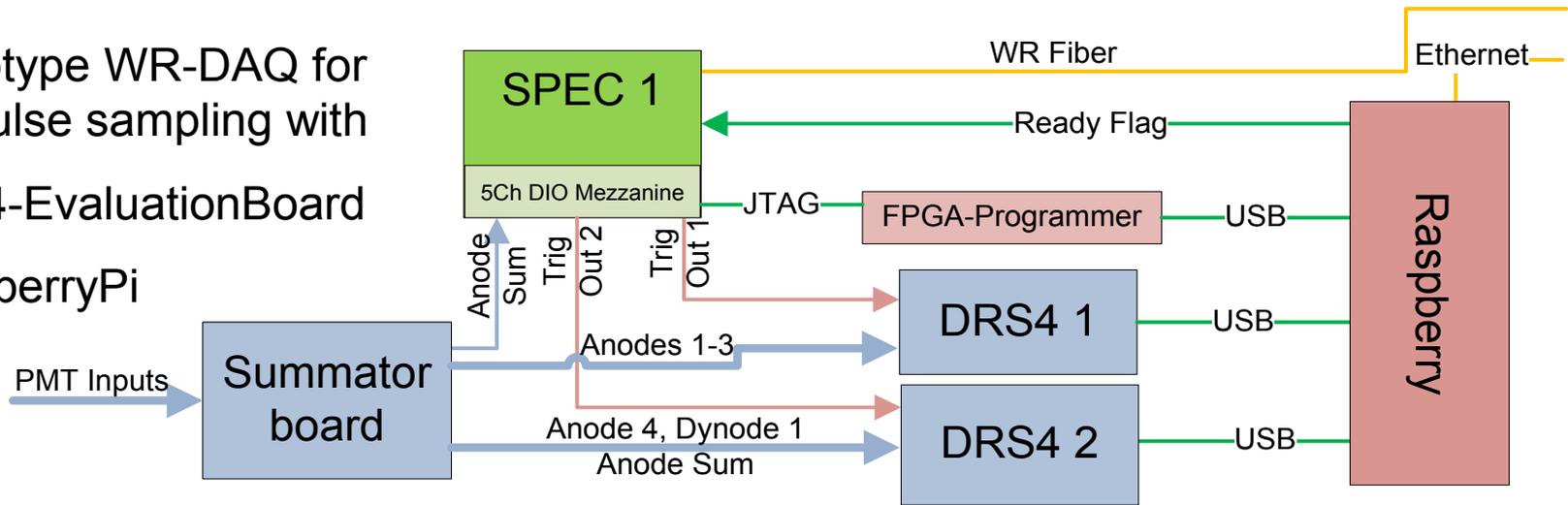
DESY adapted to CTA/HiSCORE (2012+)

- nsec-timestamping
- UDP timestamp transport
- (PPSOut/) 10MHz out
- DAQ/frontend triggering
- status monitoring, ...

# HiS-9 Station : a SPEC-based mini-DAQ

A prototype WR-DAQ for GHz pulse sampling with

- DRS4-EvaluationBoard
- RaspberryPi



## SPEC card

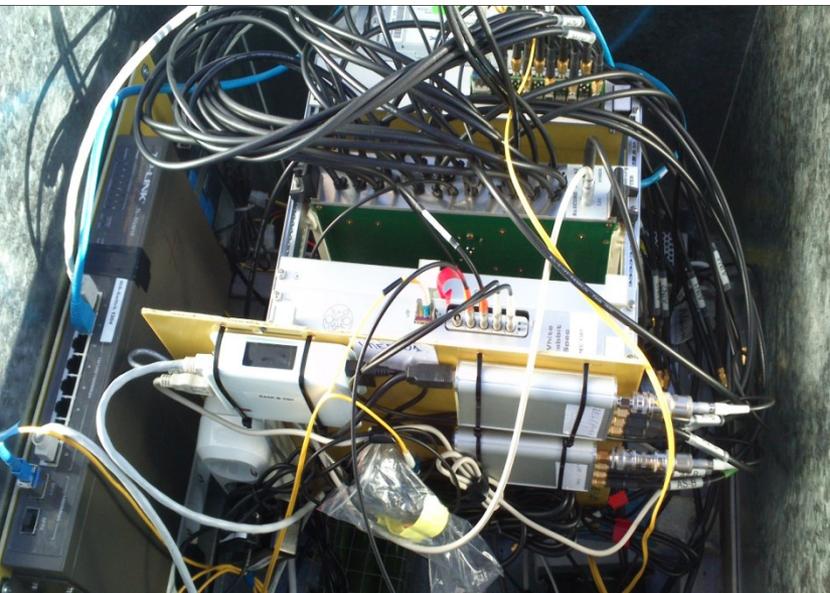
- Runs WR clock
- Stamps trigger-times + sends over WR fiber
- Transmits WR status over Ethernet

## DRS4-EB (PSI)

- Capture analog PMT signals + WR trigger pulse

## Raspberry

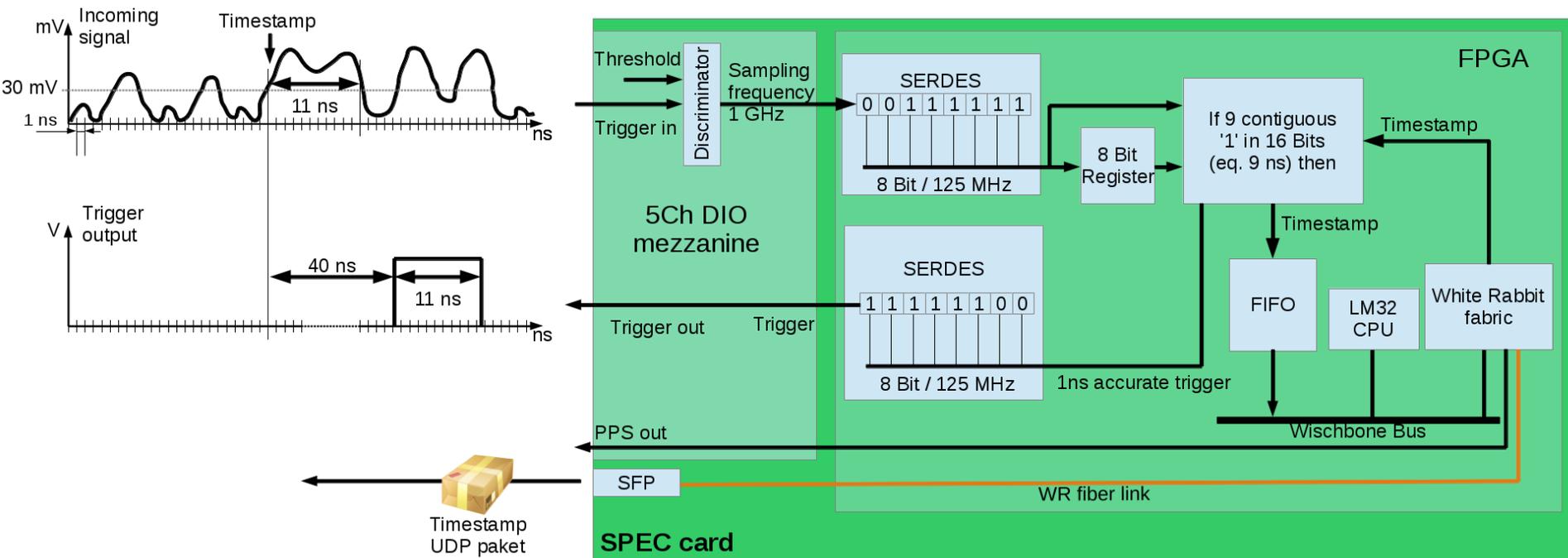
- Reads out DRS/EB board on trigger
- Uploads bulk data over a second fiber
- Programs FPGA / Backup SPEC-USB



# WR SPEC Node – the HiSCORE specific design

## SPEC FPGA modifications

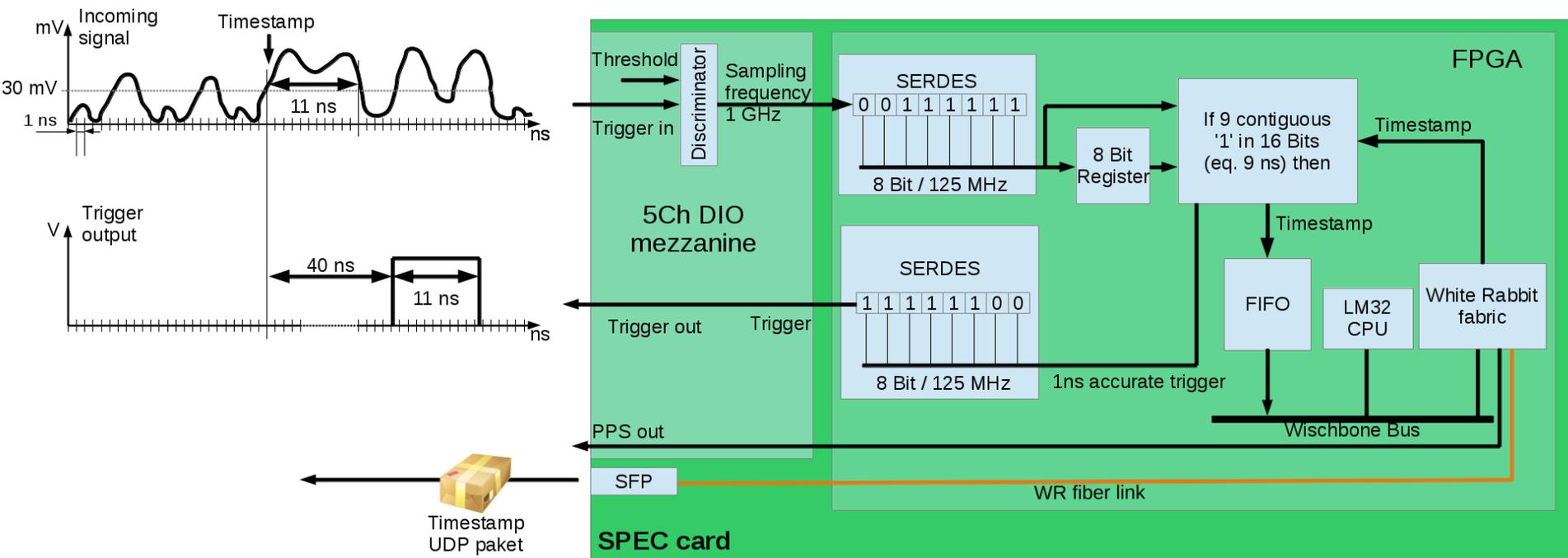
- Taking advantage of the features of the 5Ch DIO card
  - Configure some signals as input for the analog signal
  - Configure some signals as DRS4 trigger and handle Raspberry ready flag
  - Setting a threshold for incoming signals
- Using Spartan 6 SERDES blocks for deserialization



# WR SPEC node – the HiSCORE specific design (2)

## SPEC FPGA modifications

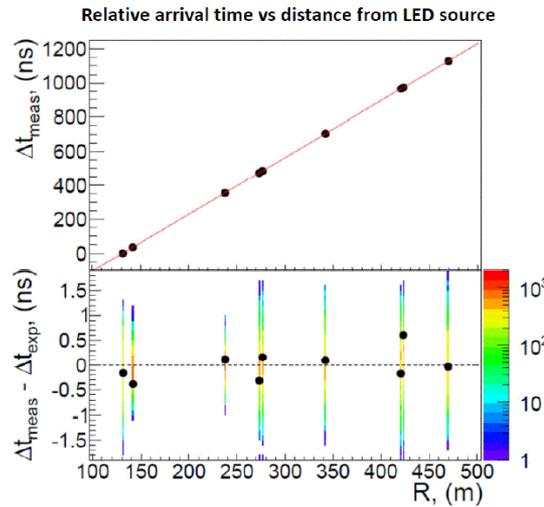
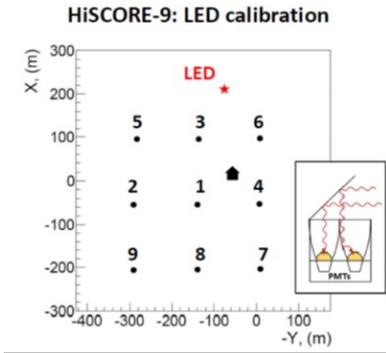
- Filter out signals shorter than 9 nsec (configurable)
- Timestamp the trigger arrival time
- Send timestamps over WR link to DAQ center (software)
- Introduce a command to adjust threshold over USB-UART



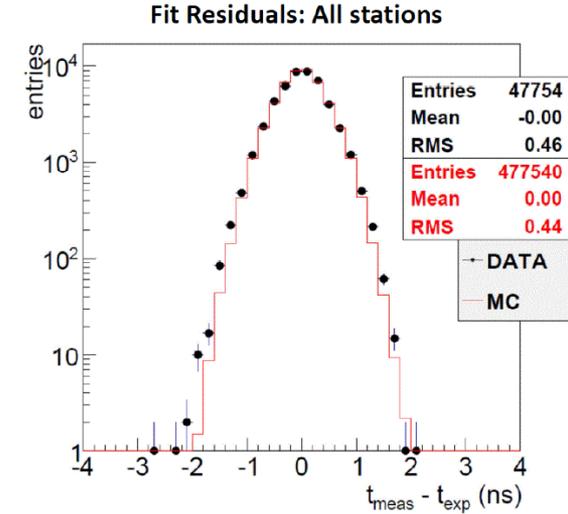
# HiSCORE-9 Results w/ WR Data only: LED and EAS

## > External LED-Calibration

Fit-Resid  $\sim 0.44$ ns



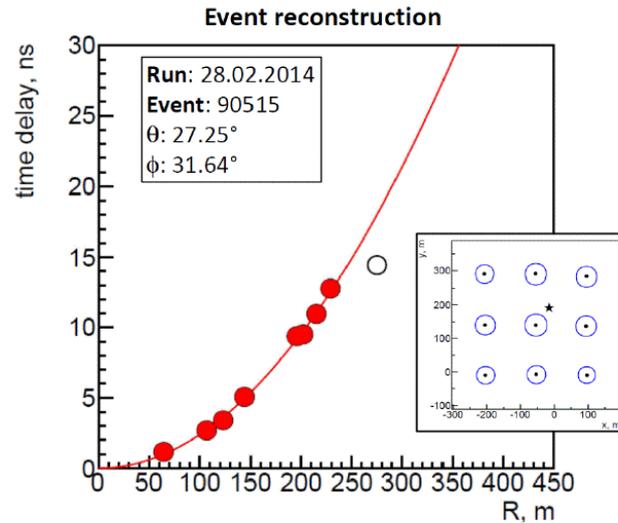
(a)



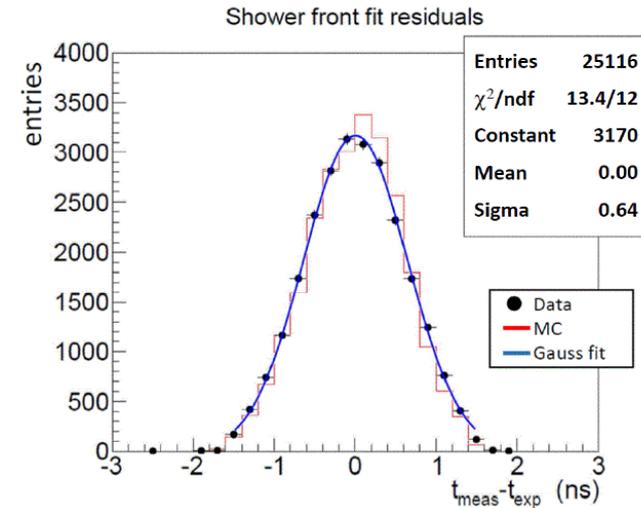
(b)

## > Cosmic Air Shower Reconstruction

Fit-Resid  $\sim 0.6$ ns



(a)



(b)

(left) Shower front: time-delay vs. radius

(right) fit-residuals all stations

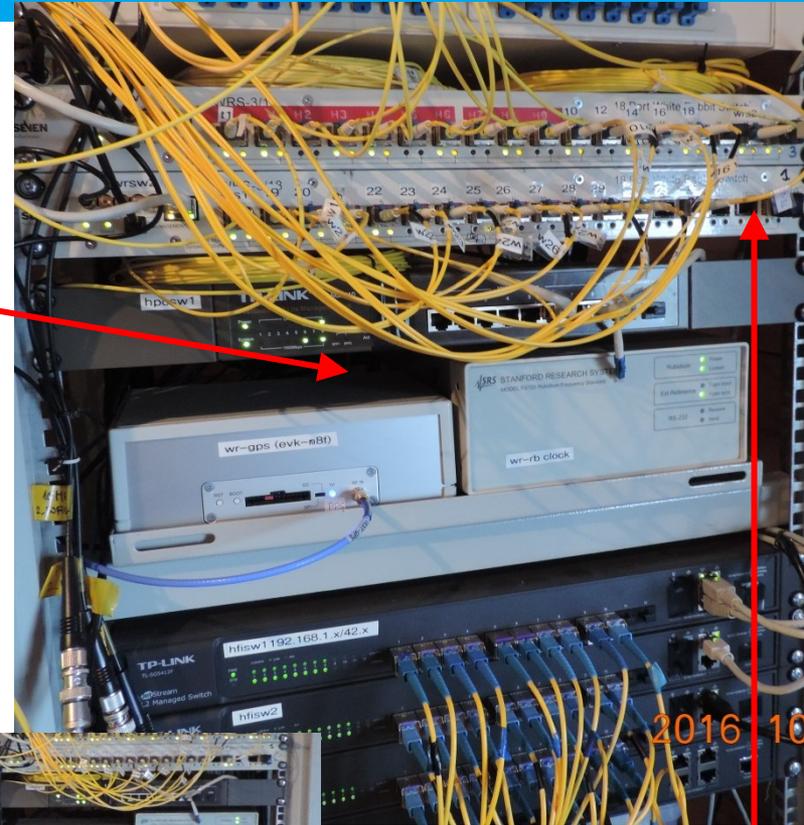
Figure 9: EAS shower reconstruction. (a) Arrival time delay vs distance from LED source. (b) Shower front fit residuals. ICRC2015, 1041

# WR ClockMaster – an end-to-end Timing Setup

> Completed the HiSCORE WR setup by a GPS-disciplined RbMaster Clock (Oct.2016)

> Central nsec-monitoring all other subsystem clocks running at the TAIGA-site by:

> WR-SPEC cards running in “nsec-TDC mode” (time-stamping)

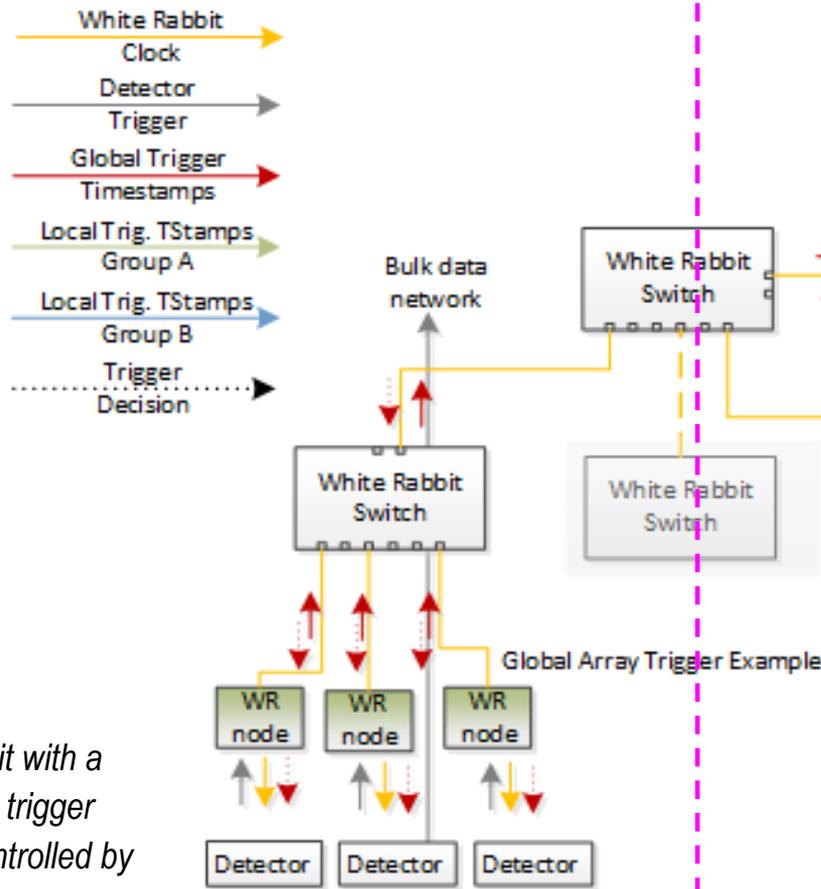


WR-Switches: GrandMasterSW  
+ BoundarySW

# A more complex WR-application (proposal) ....

# WR-driven Array Trigger Concepts

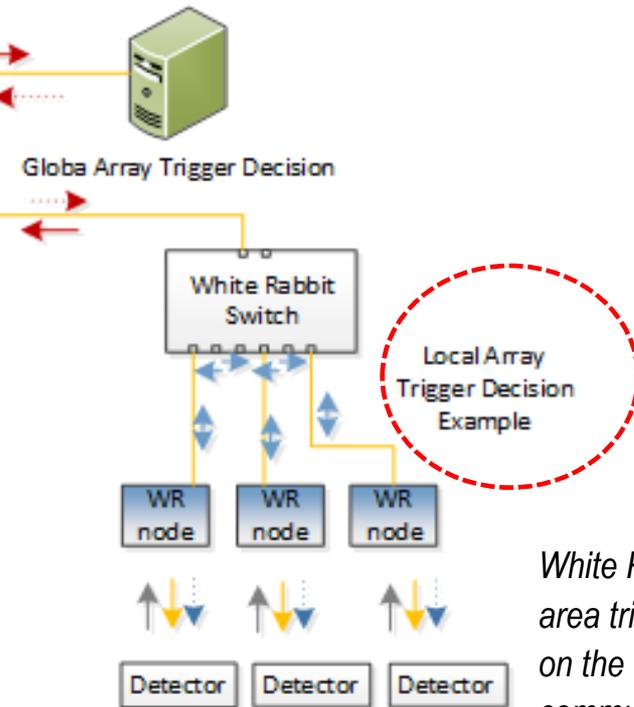
**(A) Standard application:** WR-timestamps are used to correlate the data offline



*White Rabbit with a global array trigger decision controlled by the center.*

**(B) Optional:** WR-timestamps are routed for fast online triggering and / or filtering locally. Flexible topologies.

Switch-route time packets to Array center or to relevant neighbors for central or distributed triggering.



*White Rabbit with a local area trigger decision, based on the neighbor's directly communicated trigger times.*

# Conclusions (1)

- > **Large-scale AP experiments need distributed ns-timing ...**
- > **.... WR perfectly fits requirements**
  - Clock distribution
  - Trigger time stamping
  - Active calibration ('ext. trigger')
  - In-situ-verification ( data or/and hardware redundancy )
  - ... more complex triggering
- > **WR has been implemented, and operating in HiSCORE**
  - Time-stamping
  - Operating as expected: precision, accuracy ... first physics EAS results  
( 'end-to-end test by shower' )
  - Long-term cross-checks (since 2013...)
  - Bonus: a fully WR-based GHz prototype DAQ, ready for >km<sup>2</sup>-scale
  - Timing-solution is generic – and easily adapted to other applications

# Conclusions (2)

## > Time-stamping with $\mathcal{O}(1 \text{ nsec})$

- WR-SPEC or WR-ZEN (ZynqARM-based)
- In preparation: resolution  $< 1 \text{ ns}$

## > WR-experience shapes the design of new projects: CTA + ...

- Basics methods
- Intrinsic data-redundancy (!)
- Optional self-verification (!)

## > Next: exploit the complex system-aspects, intrinsic to WR-driven DAQ's

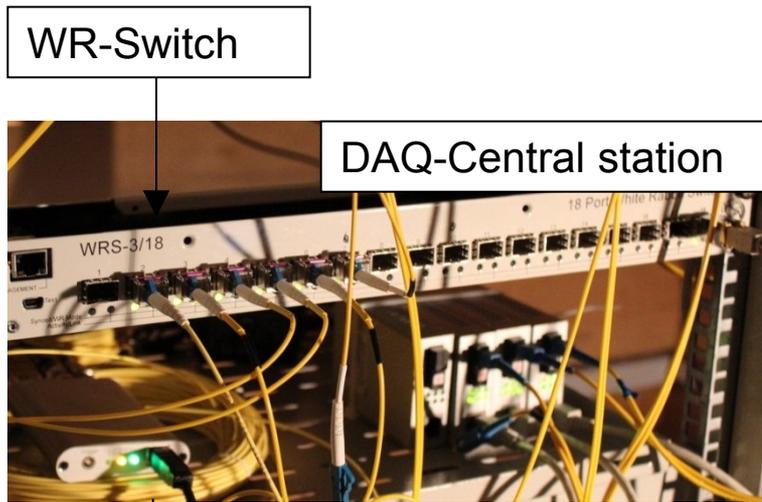
## > *Account for the unique WR-features from early stage design of new DAQ-architecture, e.g. of HAWC-South.*

*Clock, trigger-timestamping, precision calibration pulses, ...*

The DESY group is willing + interested to contribute.

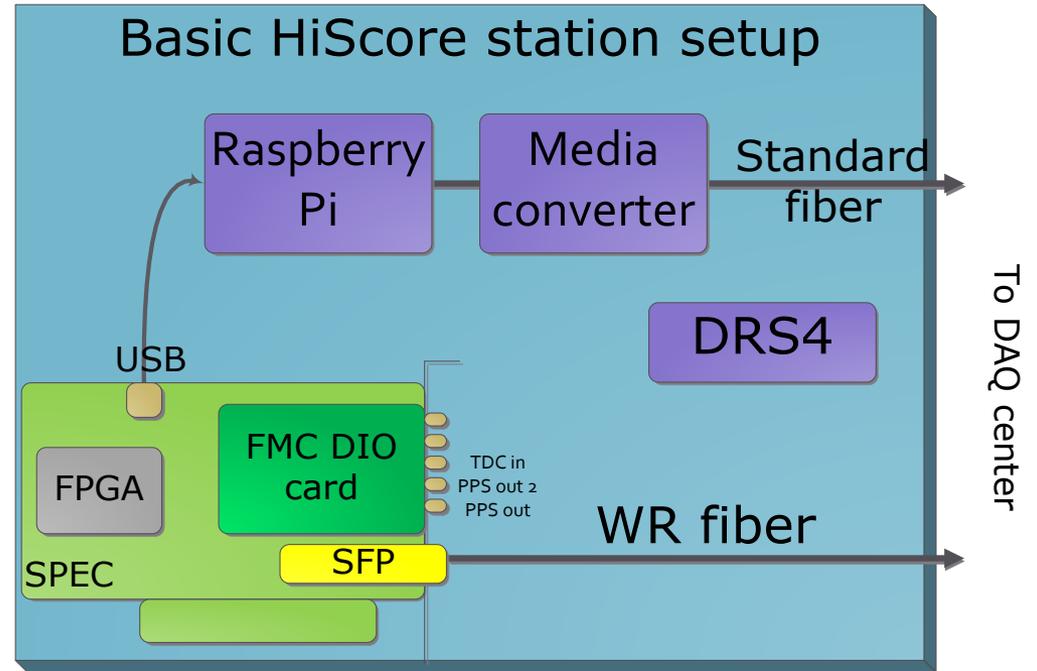
... Backup slides .

# HiSCORE setup overview



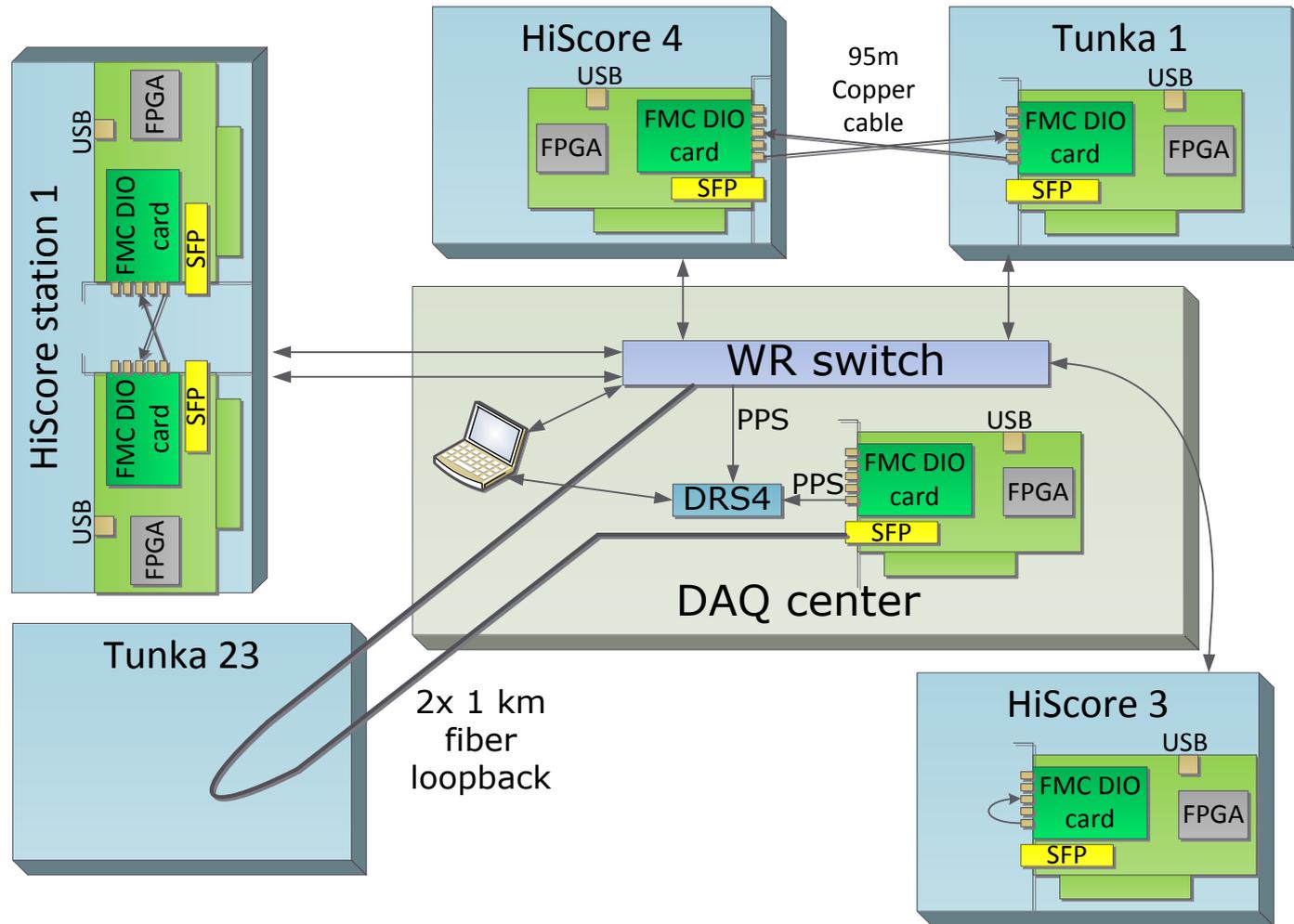
SPEC card

Raspberry Pi



- DRS4 as 5 GHz “digital scope”
- Raspberry Pi transports
  - USB Terminal
  - DRS4 (Domino Ring Sampler)
  - Temperature sensor
  - ...

# HiSCORE : WR Test-Setup 2012

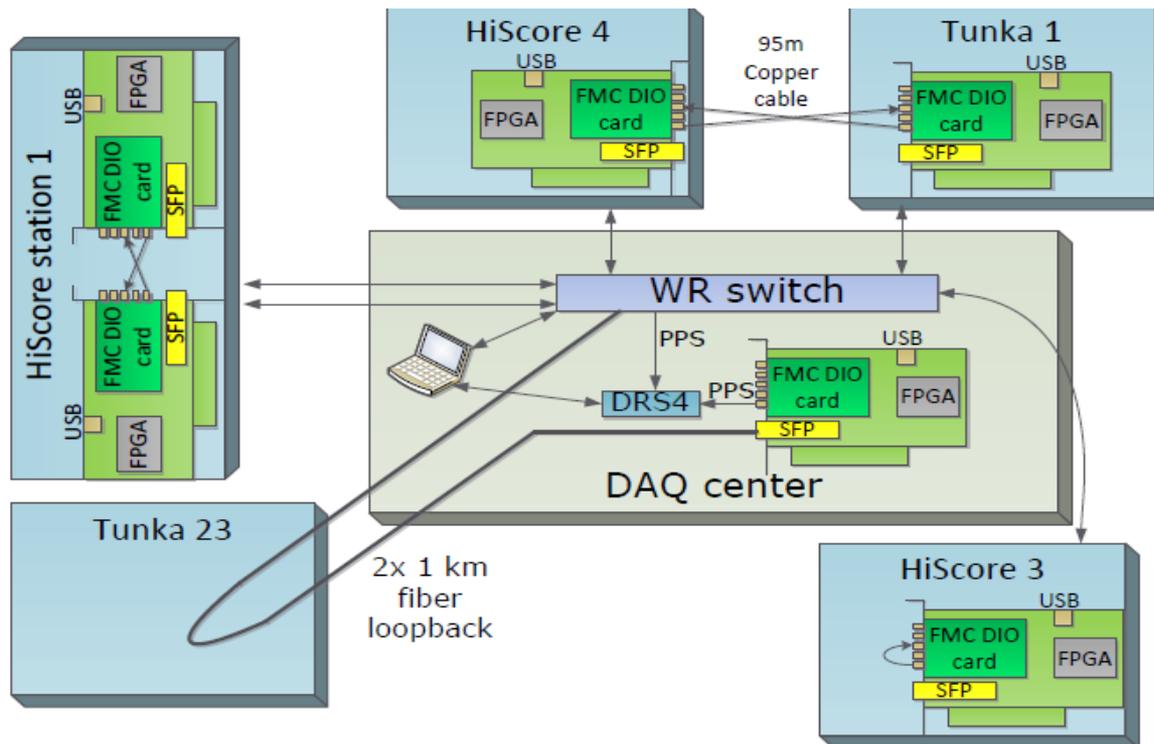


PPS signals (DIO output 1) connected to TDC-inputs (DIO input 3)

# WR – setup in Tunka

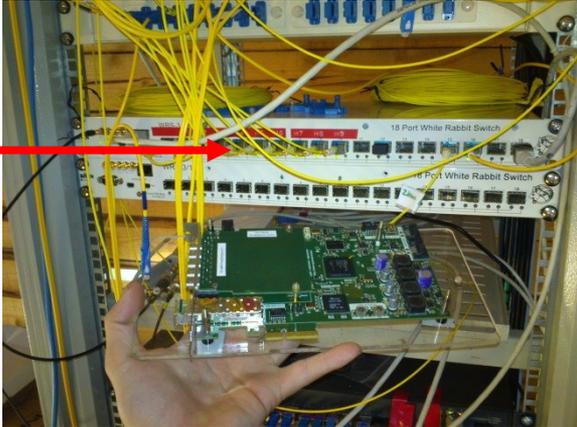
## White Rabbit Installation with a maximum of redundant cross-calibration options (October 2012 - today):

- > 2km loopback fiber cable connected to DRS4 to compare WRS and SPEC (2km) PPS clocks
- > Crosswise PPS->TDC connection to test TDC and White Rabbit
  - 2x SPEC within HiS1 station
  - 2x SPEC in 2 stations (HiS4 + Tunka-1)
- > Loopback PPS connection to test TDC performance (HiS 3)



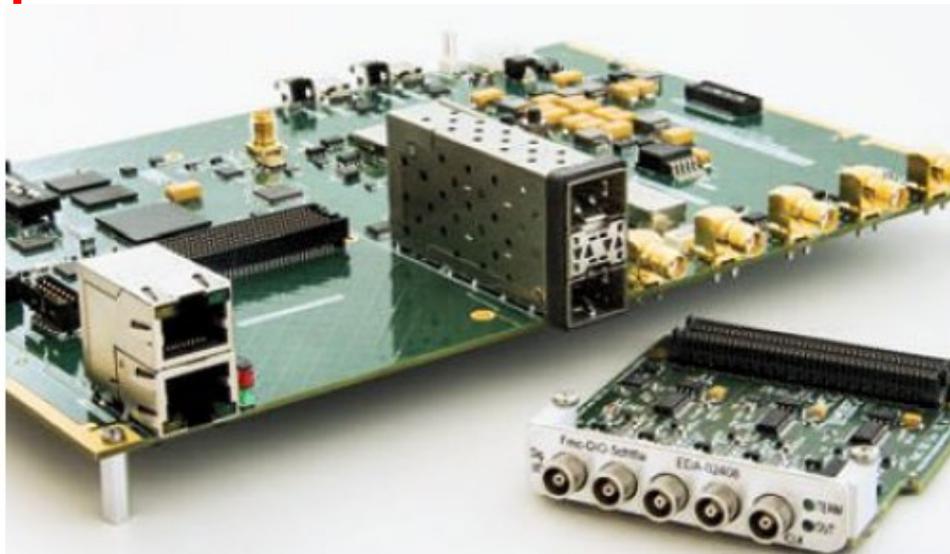
# NewTechnology: Timing with ZEN (Zynq Embedded Node)

**WR Master: WR Switch**



**1Gbit fiber**

**WR-Node: ZEN card**



## ZEN board (by SevenSols)

- Xilinx Zynq Z7015 based w/ 2x ARM9
- 1x FMC
- 2x SFP (DaisyChain, WR redundancy)
- 2x Gbit Ethernet
- Improved clock precision
- LinuxKernel

## DESY adapted for HiSCORE/CTA (2015)

- FMC-based operation (DIO, ...)
- “nsec-timestamping”
  - 2 ns now: Zynq Grade -1 (933 MHz)
  - 1 ns soon: faster Zynq by 7Sol
- TCP timestamp transport
- (( PPSOut /10MHz out ))

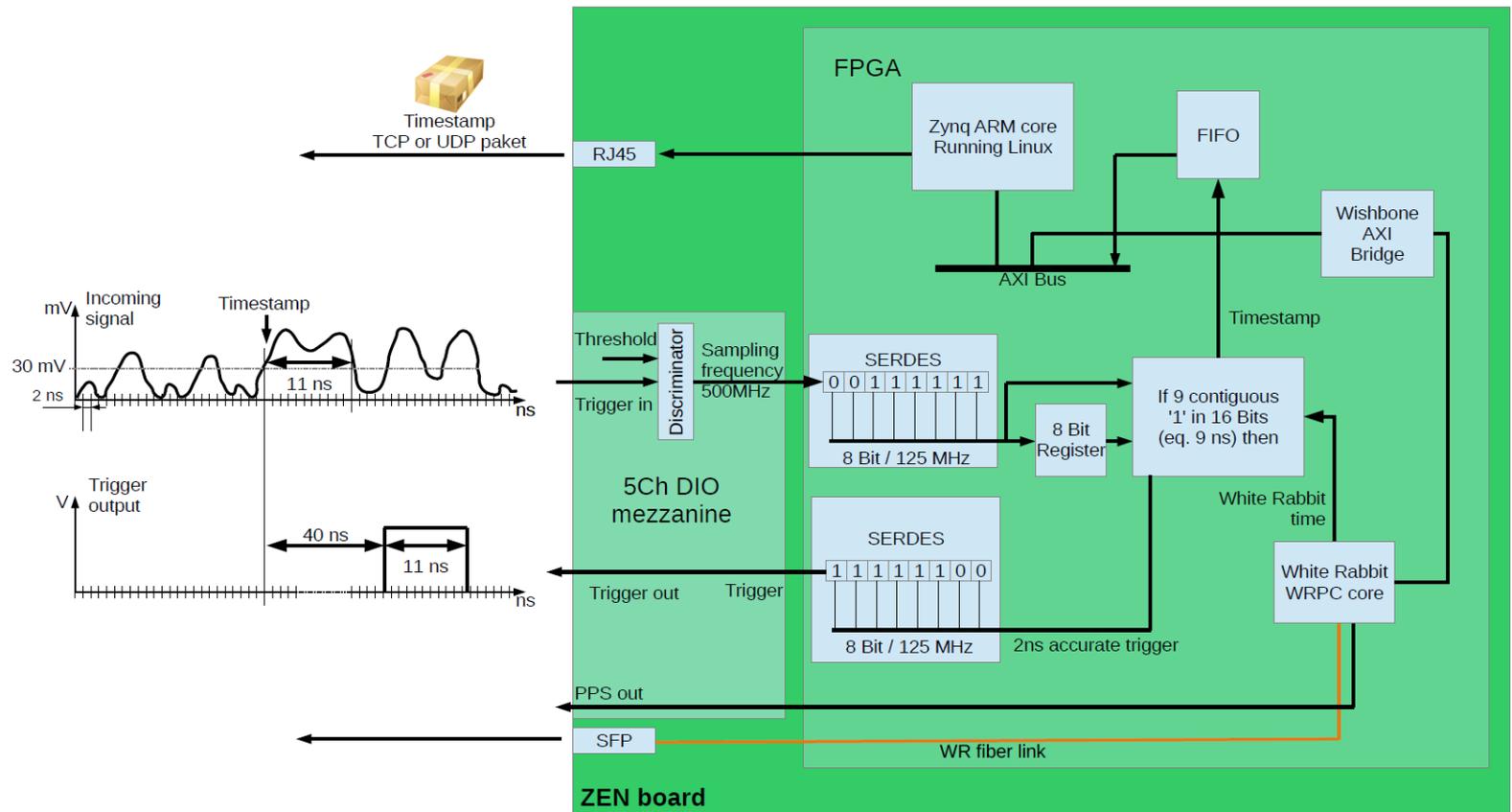
→ Performance, timing, stability, ....  
... is excellent !

# ZEN : Timestamp with Standard TDC

- > ZEN with time-stamping 2ns ( $\rightarrow$  1ns with grade -3)

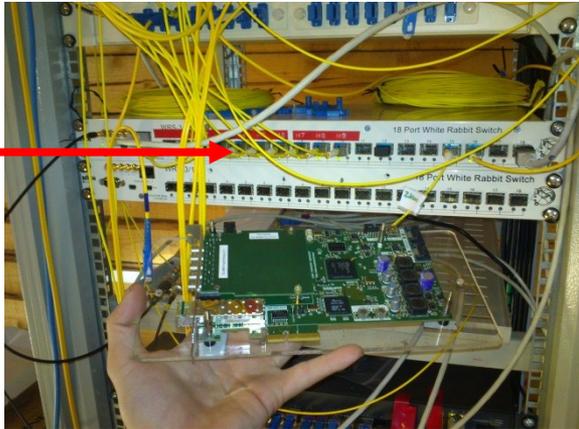
Implementation similar to our TDC on the SPEC

(w/ INPUT signal analysis, TRIGOut for local DAQ)



# ZEN : Timestamp Test

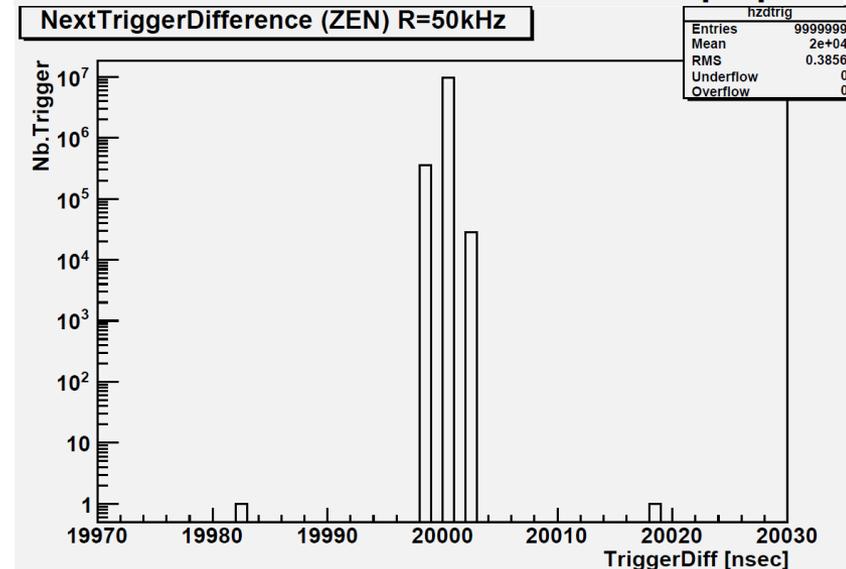
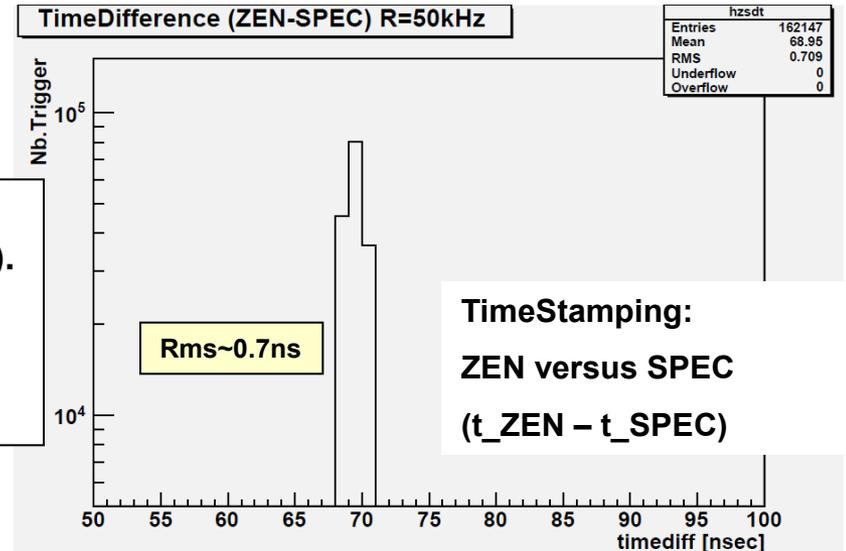
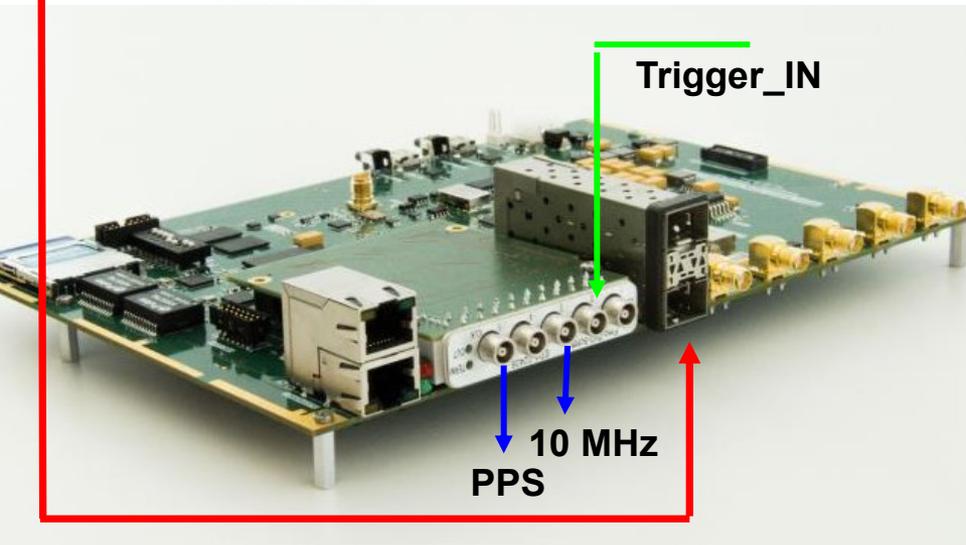
**WR Master: WR Switch**



ZEN: verifying the time-stamping (2ns).  
High trigger rate proven. ~500kHz is realistic.

**1Gbit fiber**

**WR-Node: ZEN card**



**ZEN-only test: NextTrigger Time-difference with nsec (very stable pulser).**